PATENT APPLICATION
File Number: 1042-EP

DECLARATION AND POWER OF ATTORNEY
Original Application

As below named inventor, I declare that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in this Declaration, that the information given herein is true, that I believe that I am the original, first and joint inventor of the invention entitled:

MATH COPROCESSOR

which is described and claimed in:

XX the attached specification or

___ the specification in application Serial No. _____ filed _____

that I acknowledge my duty to disclose information in accordance with 37 C.F.R. Section 1.56 and defined on the attached sheet, which is material to the examination of this application, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application and that as to applications for patent or inventor's certificate filed by me or my legal representatives or assigns in any country foreign to the United States of America, the earliest filed foreign application(s) filed within twelve months prior to the filing date of this application and all foreign applications filed more than twelve months prior to the filing date of this application, if any, are identified below.

CHECK APPROPRIATE BOX:

___ no earlier-filed foreign applications.

__ Required information as to foreign applications filed prior to the filing date of this application is on page __ attached hereto and made a part hereof.

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Name (201) NORTH, Gregory Allen	Signature	Date
Name (202) GANESHAN, Murli	Signature	Date

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Section 1.56 Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by Sections 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applications to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record of being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the application takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of patentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any considerations given to

evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

© Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent or inventor.

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APPENDIX A

DSPSC

Default: 0x00000000

Definition: DSP Status/Control

Bit Definitions:

DAID [2:0] DSP Architecture ID. This read-only value will be incremented for each revision of the overall DSP coprocessor architecture (future revisions may support multiple MAC units, dedicated 0 0 0 = First architecture.

HVID[2:0] Hardware Version ID. This read-only value will be incremented each time the hardware implementation of the architecture named by DAID[2:0] is changed, typically done in response to bugs. 0 0 0 = First version.

V Overflow Flag. Indicates that an integer operation overflowed.
0 = No overflow (reset default).
1 = Overflow.

RM[1:0] Rounding Mode. Selects IEEE 754 rounding mode.
0 0 = Round to nearest (reset default).
0 1 = Round toward 0.
1 0 = Round to -∞.
1 1 = Round to +∞.

IXE Inexact Trap Enable. Enables/disables software trapping for IEEE 754 inexact exceptions.
0 = Disable software trapping for inexact exceptions (reset default).
1 = Enable software trapping for inexact exceptions.

UFE Underflow Trap Enable. Enables/disables software trapping for IEEE 754 underflow exceptions.
0 = Disable software trapping for underflow exceptions (reset default).
1 = Enable software trapping for underflow exceptions.

OFE Overflow Trap Enable. Enables/disables software trapping for IEEE 754 overflow exceptions.
0 = Disable software trapping for overflow exceptions (reset default).
1 = Enable software trapping for overflow exceptions.

DZE Divide By Zero Trap Enable. Enables/disables software trapping for IEEE 754 divide by zero exceptions.
0 = Disable software trapping for divide by zero exceptions (reset default).
1 = Enable software trapping for divide by zero exceptions.

IOE Invalid Operator Trap Enable. Enables/disables software trapping for IEEE 754 invalid operator exceptions.
0 = Disable software trapping for invalid operator exceptions (reset default).
1 = Enable software trapping for invalid operator exceptions.

IX Inexact. Status bit that's set when an IEEE 754 inexact exception occurs (regardless of whether or not software trapping for inexact exceptions is enabled). Writing a '1' to this position clears the status bit.
0 = No inexact exception detected (reset default). Writing a '0' to this bit is ignored.
1 = Inexact exception detected. Writing a '1' to this bit clears it.

UF Underflow. Status bit that's set when an IEEE 754 underflow exception occurs (regardless of whether or not software trapping for underflow exceptions

is enabled). Writing a '1' to this position clears the status bit.
0 = No underflow exception detected (reset default). Writing a '0' to this bit is ignored.
1 = Underflow exception detected. Writing a '1' to this bit clears it.

OF — Overflow. Status bit that's set when an IEEE 754 overflow exception occurs (regardless of whether or not software trapping for overflow exceptions is enabled). Writing a '1' to this position clears the status bit.
0 = No overflow exception detected (reset default). Writing a '0' to this bit is ignored.
1 = Overflow exception detected. Writing a '1' to this bit clears it.

DZ — Divide By Zero. Status bit that's set when an IEEE 754 divide by zero exception occurs (regardless of whether or not software trapping for divide by zero exceptions is enabled). Writing a '1' to this position clears the status bit.
0 = No divide by zero exception detected (reset default). Writing a '0' to this bit is ignored.
1 = Divide by zero exception detected. Writing a '1' to this bit clears it.

IO — Invalid Operator. Status bit that's set when an IEEE 754 invalid operator exception occurs (regardless of whether or not software trapping for invalid operator exceptions is enabled). Writing a '1' to this position clears the status bit.
0 = No invalid operator exception detected (reset default). Writing a '0' to this bit is ignored.
1 = Invalid operator exception detected. Writing a '1' to this bit clears it.

APPENDIX B

Instruction Set

Notes:

1) Shaded fields in instruction encodings indicate bits that are ignored by the DSP coprocessor.
2) The <cond> portion of each instruction mnemonic refers to the standard ARM conditional mnemonic extension (see the second column of Table 15).
3) Coprocessor number 4 is associated with single and double precision floating point numbers.
4) Coprocessor number 5 is associated with 32- and 64-bit integers.
5) Coprocessor number 6 is associated with the accumulators and the DSPSC register.

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